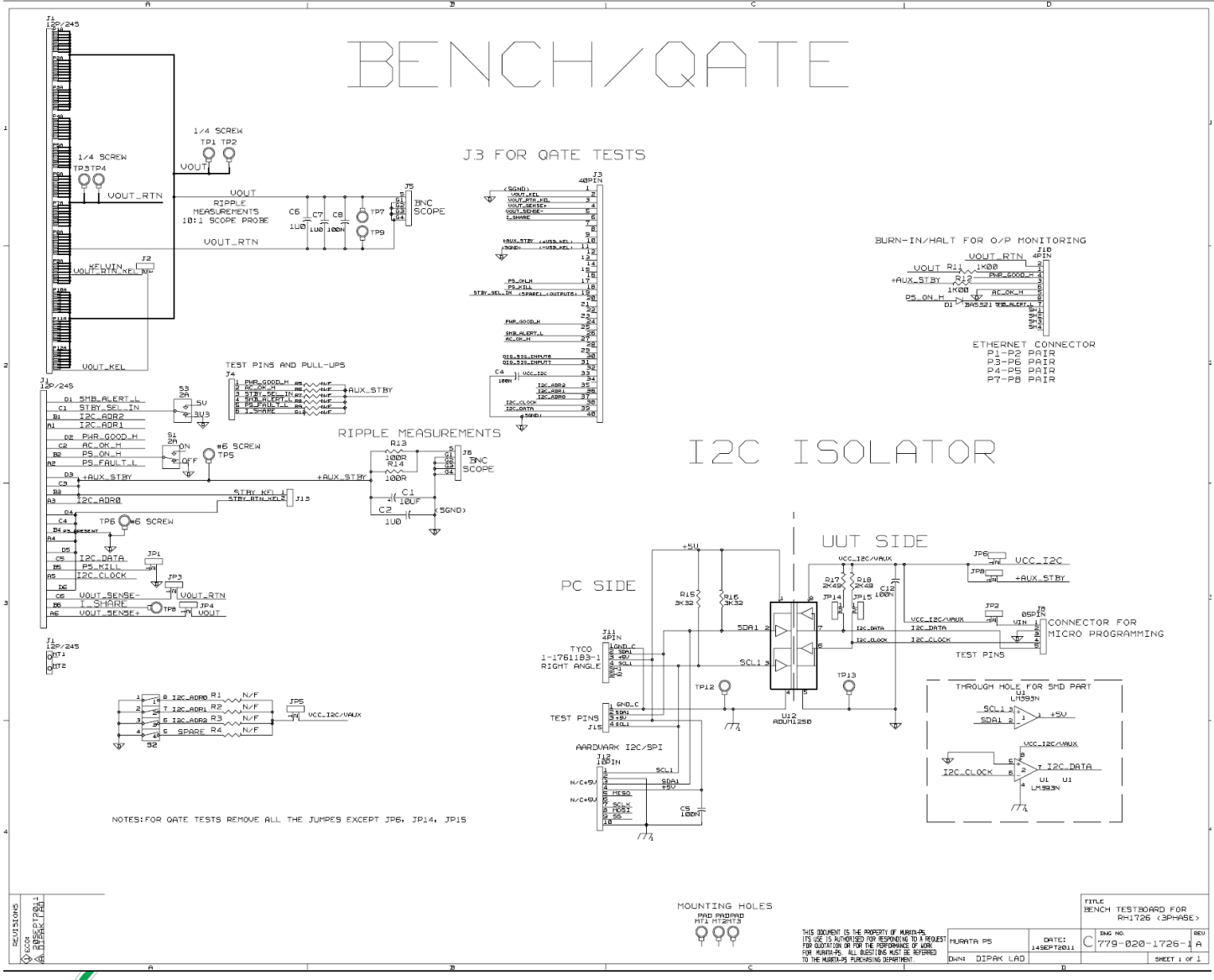
PRODUCT OVERVIEW

The D2U5T-54-CONC (8401654-1) interface connector card is intended to be used to interconnect the output voltages and signals of the D2U5T-H3-7000-54-HU4C three phase rectifier power modules for laboratory/bench level evaluation of the product. End Users can also use this card in their applications as an alternative to a power/mid or interposer plane in their host system (consult Murata Sales for details).

SAFETY PRECAUTION

The D2U5T-54-CONC output connector card is intended to facilitate the connection of the output supply rails of the power module. As such there is a high energy source (54VDC) exposed on the output connector card; please take the necessary safety precautions during the use of this connector card for product evaluation.

SCHEMATIC

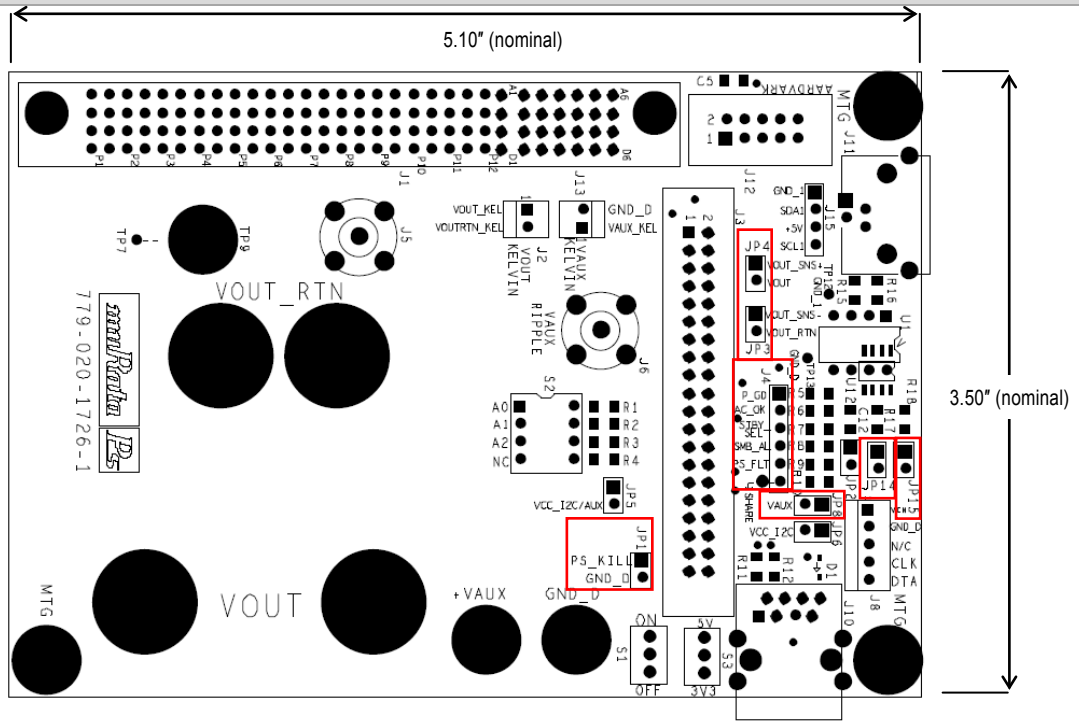


RoHS COMPLIANT

For full Details go to
www.murata-ps.com/rohs

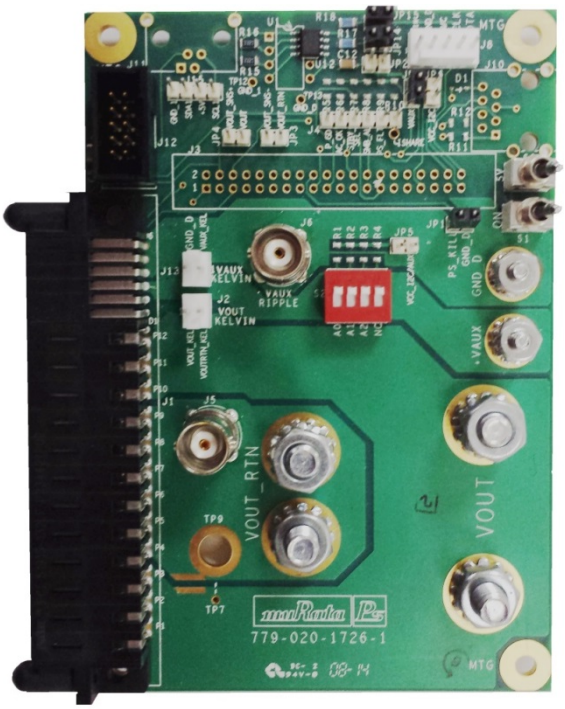
IMAGES

PCB SILKSCREEN (TOP VIEW)

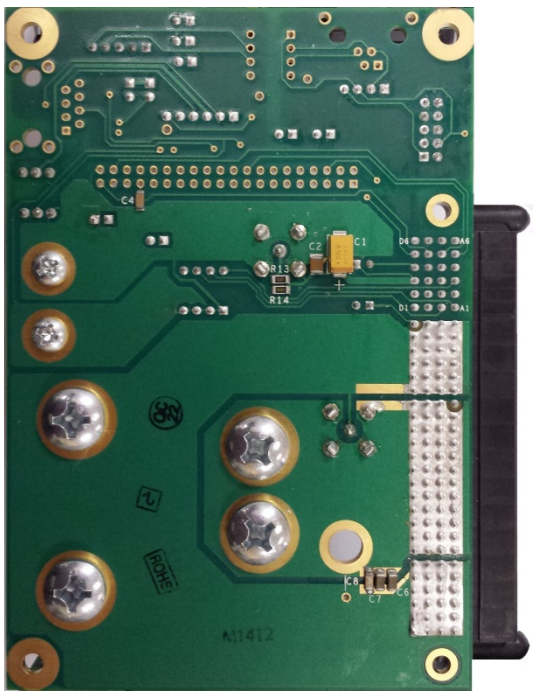


PHOTOGRAPHS

Top View



Bottom View



USER CONFIGURATION NOTES

1. Ensure that the following User Configurable jumpers have shorting headers (shunts) fitted across their respective Pins 1 & 2 (refer to schematic):
   a) JP1 (PSKILL to STBY_RTN)
   b) JP3 & JP4 (Local Sense connections; JP3 VOUT_SENSE- to VOUT_RTN; JP4 VOUT_SENSE+ to VOUT)
   c) JP8 (+AUX_STBY connection)
   d) JP14 (U12 Pin 7 I2C_DATA) & JP15 (U12 Pin 6 I2C_CLK); pull up resistors for respective pin to +AUX_STBY (via JP8)

2. The BNC connectors for ripple & noise measurements of AUX_STBY (J6) and VOUT (Main 54V output) are intended for direct (BNC to BNC) connection (or via a 10X probe if required) to an oscilloscope (note that J6 has a series 50ohm resistance - see schematic).
   Note also that the measurement node is filtered with a parallel connected 10µF tantalum and 1µF ceramic capacitor (across tip to ground); the measurement bandwidth shall be limited to 20MHz.

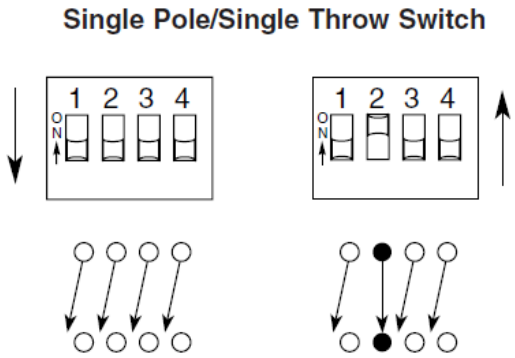
3. Connector J11 is a Total Phase Aardvark I²C/SPI compatible interface connector. The "Aardvark" external device allows communications via a USB port of a laptop or PC that can be used with the proprietary Aardvark Control Centre™ software GUI. The interface to the power module is buffered via an I²C Isolator device (Analog Devices ADµM1250) that is connected to J11 (see schematic). This device (U12) isolates and level shifts the Serial Clock (SCL) and Serial Data (SDA) lines respectively to facilitate trouble free communication.

4. Three (3) User Configurable switches are provided:
   a) S1 toggles the PS_ON Signal to allow the User to readily turn on/off the Main 54V DC output; the switch is annotated "ON" and "OFF"; toggling the switch between these positions turns the Main output on/off accordingly.
   b) The rectifier power module has selectable +AUX_STBY voltage rail being either 3.3V or 5V.
      S3 toggles the STBY_SEL_IN signal line to select the appropriate +AUX_STBY voltage; the switch is annotated "3V3" and "5V" and toggling the switch between these positions selects the appropriate voltage.
      The position of S3 should be selected before the application of AC power to the rectifier; it is not recommend toggling S3 between the 3.3V and 5V positions while the rectifier is operational.
      Toggling from the 3.3V to 5V setting while operational shall cause the +AUX_STBY to initiate an OVP of the output.
      Toggling the 5V to 3.3V setting while operational shall cause no damage to the rectifier; however the output will revert to 3.3V operation and this may have an undesired effect if powering End User electronics.
   c) S2 is a four (4) position DIL switch that is intended to select the User configurable bits that assign the variable address for I2C communications with the rectifier.
      Note that address bits A0, A1, & A2 are internally connected by a 10K ohm pull up resistor to VDD (either 3.3V or 5V dependent upon the selection of S3).
      The required address should be set before power is applied to the rectifier (no change of address is possible while power is applied).

S4 Position #3 (A2) (Serial Address BIT 2)	S4 Position #2 (A1) (Serial Address BIT 1)	S4 Position #1 (A0) (Serial Address BIT 0)	Power Module Main Controller (Serial Comm Slave Address)	Power Module Main EEPROM (Serial Comm Slave Address)
LOW	LOW	LOW	0xB0	0xA0
LOW	LOW	HIGH	0xB2	0xA2
LOW	HIGH	LOW	0xB4	0xA4
LOW	HIGH	HIGH	0xB6	0xA6
HIGH	LOW	LOW	0xB8	0xA8
HIGH	LOW	HIGH	0xBA	0xAA
HIGH	HIGH	LOW	0xBC	0xAC
HIGH	HIGH	HIGH	0xBE	0xAE

The address convention uses 7-bit left shifted Slave Device addressing with the Read/Write bit either a "0" (Write) or a "1" (Read). The addresses above assume the Read/Write bit is a "0".

S4 operation is shown in the diagram opposite (also refer to the schematic).
With any of the DIL switches (1, 2, & 3) set to the "off" (open) position, the corresponding address line (A0/A1/A2) shall be set to a logic level high (by action of the internal 10K ohm pull up resistor.
Operating the appropriate switch to the "on" (closed) position will connect the appropriate line to a logic level low.
Note: The switch position DIL Position #4 is unused and has no connection (NC) on the connector card.



USER CONFIGURATION NOTES

5. If required connector J4 can be used to monitor the status of I/O signals generated by the rectifier power module. Each pin is internally connected by a 10K ohm pull up resistor to VDD (either 3.3V or 5V dependent upon the selection of S3).
   The following table shows the pin assignments for the relevant signals and their description.

Signal (I/O)	Description
PS_ON_H (Input)	Internal 10K pull-up resistor to internal VDD. • Leaving signal pin open = Main Output ON • Tying signal pin to GND = Main Output OFF.
PS_KILL (Input)	Short pin; internal 10K pull-up resistor to internal VDD. • Leaving signal pin open = All Outputs off • Tying signal pin to GND = All Outputs enabled.
PS_FAULT_L (Output)	Internal 10K pull-up resistor to internal VDD. • PSU Fault Status
PWR_GOOD_H (Output)	Internal 10K pull-up resistor to internal VDD. • Main Output Status OK
I_SHARE (Input/output -bus)	Analog representation of main output current; can be left open if not used.
STBY_SEL_IN (Input)	Internal 10K pull-up resistor to internal VDD. • Leaving signal pin open = +5V STBY • Tying signal pin to GND = 3V3STBY
AC_OK_H (Output)	Internal 10K pull-up resistor to internal VDD. • AC OK Status
SMB_ALERT_L (Output)	Internal 10K pull-up resistor to internal VDD. • SMB Alert signal output

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